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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,101	10/28/2003	Andras Szabo	010262-014410US	6613

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EXAMINER	
BUDD, PAUL A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/696,101	SZABO ET AL.
	Examiner	Art Unit
	Paul A. Budd	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1 and 5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

a) Page 6, line 17, change "one" to the corrected - - on - -,

b) Page 8, line 31, change "input pads 314, 324, and 334" to the corrected - - Input pads 312, 326, and 336 - -,

c) Page 9, line 15, the phrase "increase as the on transistors 310, 320, and 330," makes no sense, change this to - - increase as the transistors 310, 320, and 330 turn on - -.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims **1,7** recite the limitation "sufficiently long duration". There is no defined standard for this limitation and it is considered vague and indefinite. For the purposes of this office action the inherent delay defined by the claimed device structure is considered to be sufficient to meet the claimed device. It is the claimed structure that determines this delay.

Claims **5,6** recite the limitation "trimming circuit" in the beginning of the dependent claim. There is insufficient antecedent basis for this limitation in these

claims or claim **1**. For the purposes of this office action the term "delay transistor" will be used in place of "trimming circuit".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1-6** are rejected under 35 U.S.C. 102(b) as being anticipated by Stein et al. (US Patent 4,725,747).

Regarding claim **1**, Stein teaches a delay transistor [FIG. 1, 12] comprising:

a substrate [column 2, lines 6-7];

a plurality of conduction channels [FIG. 2, 50; the channel under the gates for sub-transistors 21a-21j, column 7, lines 2-3] embedded in the substrate;

a plurality of active regions [FIG. 1, 20a-20e (drains), 18a-18f (sources)] embedded in the substrate, the active regions alternating with the conduction channels [see FIG. 1];

a source contact [22, column 3, lines 22-23] coupled with first alternating active regions [20a-20e, 18a-18f];

a drain contact [22, column 3, lines 22-23] coupled with second alternating active regions; and

a gate structure [16] overlaying the conduction channels [as above], the gate structure [16] being configured to receive an input signal [see FIG. 1], wherein the gate structure is a single [see FIG. 1, column 3, lines 16-21] gate structure, and

wherein the gate structure provides an RC delay [column 5, lines 6-14] to the input signal and filters power [column 2, lines 8-16] and voltage spikes [column 1 lines 57-64] in the input signal, the RC delay being of a sufficiently long duration so as to decrease the switching speed of the transistor and allow the gate structure to filter power and voltage spikes.

Regarding claim **2**, Stein teaches the delay transistor of claim 1 wherein the gate structure has a serpentine shape [column 2, lines 29-32].

Regarding claim **3**, Stein teaches the delay transistor of claim 1 wherein the gate structure comprises polysilicon [column 3, lines 12-13 & lines 26-27].

Regarding claim **5**, Stein teaches the *delay transistor* of claim 1 wherein the delay transistor is an NMOS transistor [FIG. 1; 14; column 3, lines 26-27].

The gate structure is 24, the drain or source contacts are 30, and the plurality of active regions are the sources 26a-26d and drains 28a-28c.

Regarding claim **6**, Stein teaches the *delay transistor* of claim 1 wherein the delay transistor is a PMOS transistor [FIG. 1; 12; column 3, lines 12-13].

2. Claims **8-11** are rejected under 35 U.S.C. 102(b) as being anticipated by Alter (US Patent 5,589,702).

Regarding claim **8**, Alter teaches a delay pad structure [FIG. 2] comprising:

a substrate [FIG. 2, 15];

an active region [FIG. 2, 18] embedded in the substrate [15], and active region being configured to receive an input signal [26], the active region [18] having a serpentine shape [see FIG. 2, column 3, lines 44-45], the active region [18] providing an RC delay to the input signal and filtering power and voltage spikes in the input signal; and

a plurality of diodes coupled with the active region [18], the diodes being reversed biased, wherein the diodes provide additional capacitance to the RC delay.

A diffused resistor embedded in a substrate is inherently also a reversed biased diode (if forward biased it no longer functions as a resistor). A serpentine diffused resistor inherently discloses additional diode capacitance since the

junction area of the diffused diode can be adjusted to obtain whatever capacitance is needed without affecting the resistance of the resistor. A diffused resistor made up of contiguous squares (with Ohms per square) which can be small squares or larger squares having the same resistance but different capacitances.

Regarding claims **9-10**, Alter teaches the delay pad structure [FIG. 2] of claim 8 comprising:

wherein the substrate is a p-type substrate [column 4, lines 57-60] and wherein the active region is an n+ region [column 4, lines 57-60].

Regarding claim **11,** where "the delay pad structure of claim 8 wherein the delay pad structure is used in a trimming circuit for modifying electronic circuits." Please refer to "In re Pearson 181 USPQ 641 (CCPA)" with regards to this claim. The intended use of the pad delay structure does not avoid prior art.

2. Claims **12-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Yao et al. (US Patent 4,937,639).

Regarding claim **12**, Yao teaches a delay line structure [FIG. 7 & 10-11] comprising:

a substrate [51];

a thin oxide layer [FIG. 7 & 10-11, 63] coupled onto a first side of the substrate [51], the thin oxide layer [63] having a square shape;

a polysilicon layer [FIG. 10, 64] coupled onto the thin oxide layer [63], the polysilicon layer [64] being configured to receive an input signal [66], the combination of the thin oxide layer [63] coupled between the substrate [51] and the polysilicon layer [64] providing an RC delay to the input signal and filtering power and voltage spikes in the input signal [column 8, lines 3-30]; and

a plurality of diodes [FIG. 10, 71, 73 and 58a-53-51] coupled with the polysilicon layer [64], the diodes being reversed biased, wherein the diodes provide additional capacitance to the RC delay.

Regarding claim **13**, Yao teaches a delay line structure FIG. 7 & 10-11] of claim 12 wherein the substrate is a p-type substrate. Column 9, line 21, claim 1 Yao claims a "semiconductor substrate of a first conductivity type", which teaches either an n-type or p-type substrate.

Regarding claim **14**, as above with respect to claim 11 please refer to "In re Pearson 181 USPQ 641 (CCPA)". The intended use of the pad delay structure does not avoid prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **4,7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Stein et al. (US Patent 4,725,747) in view of Matsuo el al. (US Patent 5,744,838).

Regarding claim **4**, Stein teaches all the limitations of claim **1** [FIG. 1, 14] as above wherein the delay transistor further comprises a plurality of *transistors* [40] coupled with the single gate structure, wherein the *transistors* contribute additional capacitance to the RC delay.

However Stein does not teach a plurality of diodes in place of the plurality of transistors. Matsuo does teach a plurality of diodes connected to a gate [FIG. 23, 106, 107,column 1-2, lines 58-3] in place of the plurality of transistors. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a plurality of diodes in order to "prevent a gate oxide film of the initial input stage logic circuit from deterioration or breaking by reducing the absolute value of the surge voltage" [column 1-2, lines 68-3], or to increase gate capacitance.

Regarding claim **7**, Stein teaches a delay stage transistor [FIG. 1, 14] comprising:

a plurality of transistors [FIG. 1, 29a-29f] coupled in parallel, each transistor being coupled between a first voltage potential [FIG. 1, Vcc (coupled through 12)] and a second voltage potential [FIG. 1, ground]; and

a plurality of *transistors* [40] coupled between the gates [29a-29f] of the transistors and the second voltage potential [ground], the gates being formed by a single gate structure [the serpentine gate 24], wherein the combination of the gate and the diodes provide a distributed RC delay [as above] to the input signal and filters power and voltage spikes in the input signal, the RC delay being of a sufficiently long duration so as to decrease the switching speed of the transistor and allow the gate structure to filter power and voltage spikes.

However Stein does not teach a plurality of diodes in place of the plurality of transistors. Matsuo does teach a plurality of diodes connected to a gate [FIG. 23, 106, 107,column 1-2, lines 58-3] in place of the plurality of transistors. It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a plurality of diodes in order to "prevent a gate oxide film of the initial input stage logic circuit from deterioration or breaking by reducing the absolute value of the surge voltage" [column 1-2, lines 68-3] or to increase gate capacitance.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Yamaguchi et al. (US Patent 6,274,908), Waggoner et al. (US

Patent 6,218,706), Tango (US Patent 4,288,829), Ferry et al. (US Patent 5,146,306), and Chang et al. US Patent (6,617,649). Also see attached 892 form for these pertinent art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEROME JACKSON
PRIMARY EXAMINER